

Fig. 1

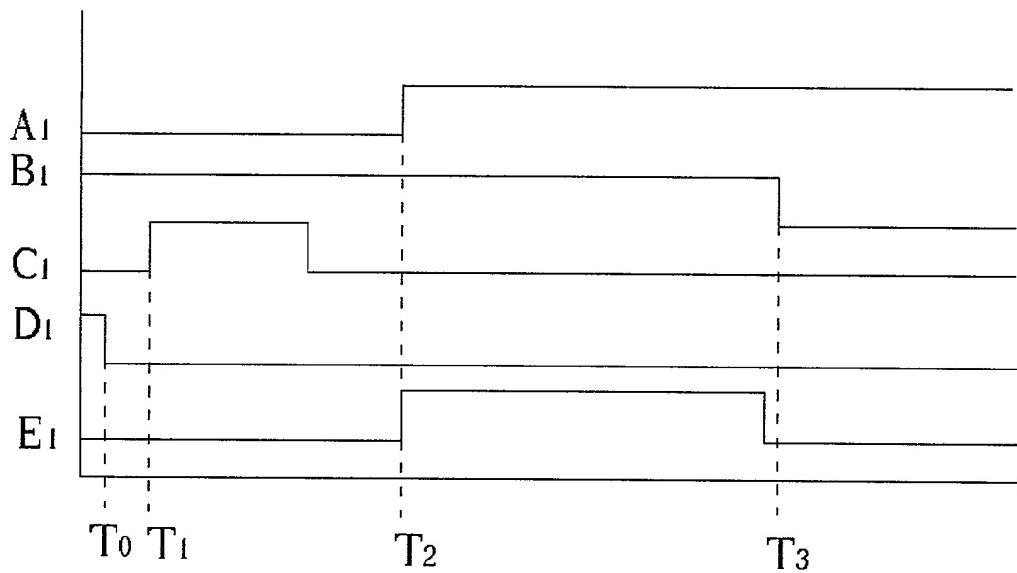


Fig. 2

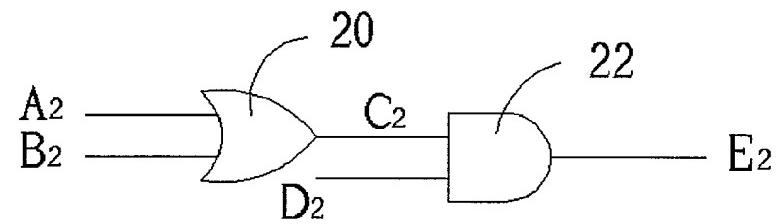


Fig. 3

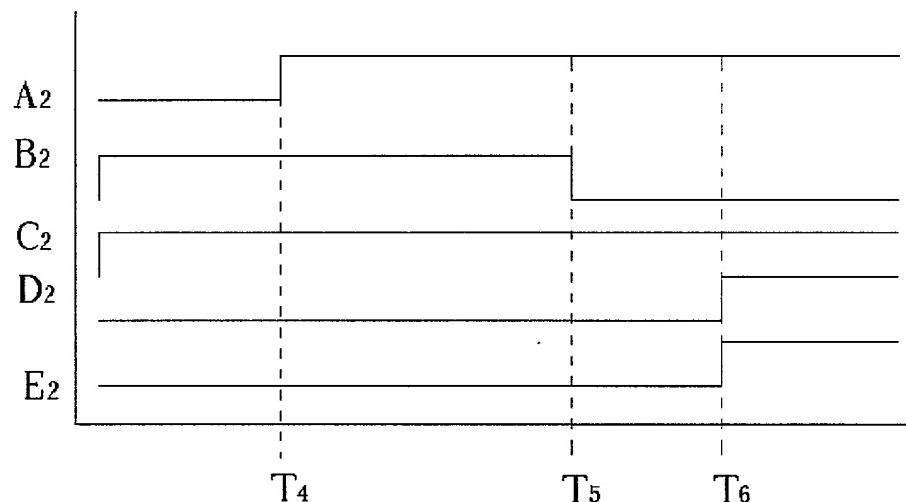


Fig. 4

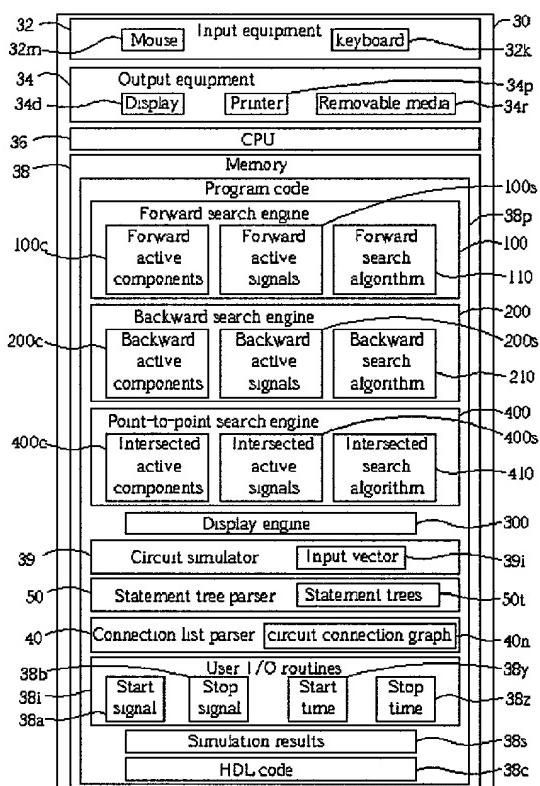


Fig. 5

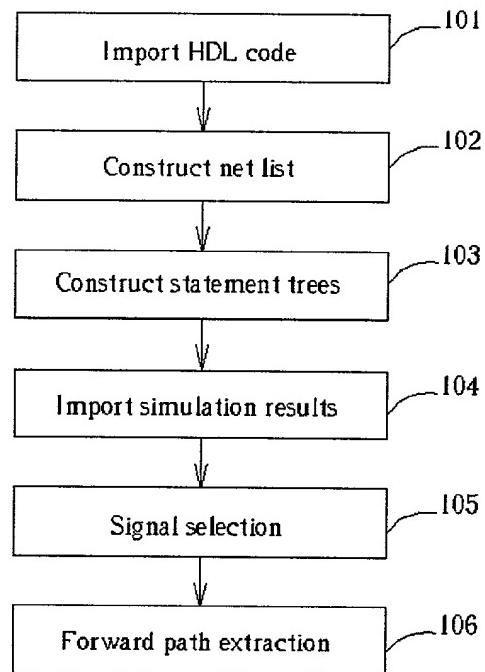


Fig. 6

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1 module
example(clk,reset,controlc,controld,controli,ind,in,ing,inh,in1,outf,outg,outh),
2: input clk,reset,ind,in,ing,inh,in1,outf,outg,outh,
3: input controlc,controld,controli;
4: output outf,outg,outh,
5: wire controlc,controld,controli,
6: wire ind,in,ing,inh,in1;
7: wire outf;
8: reg outh,outf;
9: wire sigc,sigd,sigh,sigf,sigg,sigi;
10: reg siga,sigb,sigd,sigf,sigg,sigi;
C7 11: assign outf= siga & sigb;
C1 12: assign sigc = ine | ing;
C3 13: assign sigh = sigi & in1;
C8 14: assign sigf = ine & inh;
15.
C9 16: always @(posedge clk or posedge reset)
17: begin
18:   if (reset)
19:     outh = 0;
20:   else if (controlc || controld)
21:     outh = #1 sigh;
22:   else if (!controli)
23:     outh = #1 ing;
24: end
25.
C11 26: always @(posedge clk or posedge reset)
27: begin
28:   if (reset)
29:     sigf = 0;
30:   else if (controld)
31:     sigf = #1 ind | inh;
32:   else if (!controli)
33:     sigf = #1 ing;
34: end

```

Fig. 7A

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C6  35 always @(posedge clk or posedge reset)
36 begin
37     if(reset)
38         outg = 0,
39     else if(controlc)
40         outg = sigc,
41     else
42         outg = sigc,
43 end
C2  44 always @(posedge clk or posedge reset)
45 begin
46     if(reset)
47         sigd = 0,
48     else if(controlc || controld)
49         sigd = #1 ind;
50     else if(!controlc)
51         sigd = #1 sigc;
52 end
C5  53: always @(posedge clk or posedge reset)
54 begin
55     if(reset)
56         siga = 0;
57     else if(controlc)
58         siga = #1 sigd,
59     else
60         siga = #150 sigf,
61 end
C4  62: always @(posedge clk or posedge reset)
63 begin
64     if(reset)
65         sigb = 0;
66     else if(controlc && !controld)
67         sigb = #1 sigc,
68     else if(controlc)
69         sigb = #1 sigg,
70 end

```

Fig. 7B

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C10  71: always @(posedge clk or posedge reset)
72: begin
73:   if (reset)
74:     sigg = 0;
75:   else if (controlc && !controld)
76:     sigg = #1 ini;
77:   else if (controle)
78:     sigg = #1 inh;
79: end
C12 80: always @(posedge clk or posedge reset)
81: begin
82:   if (reset)
83:     sigi = 0;
84:   else
85:     sigi = #1 inh;
86: end
87: endmodule
```

Fig. 7C

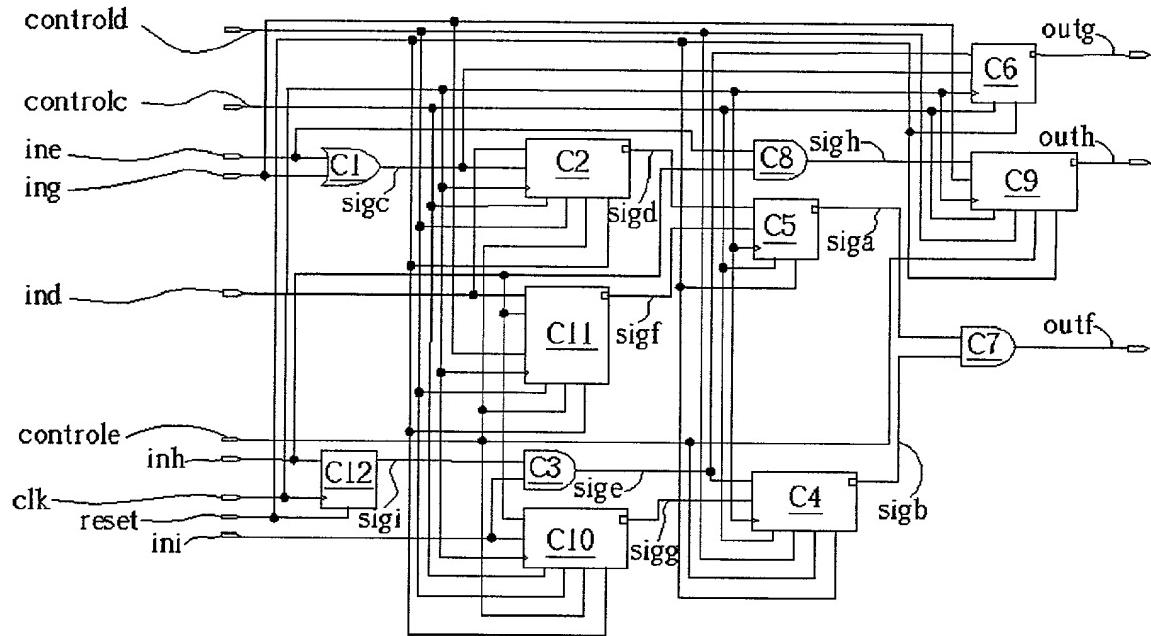


Fig. 8

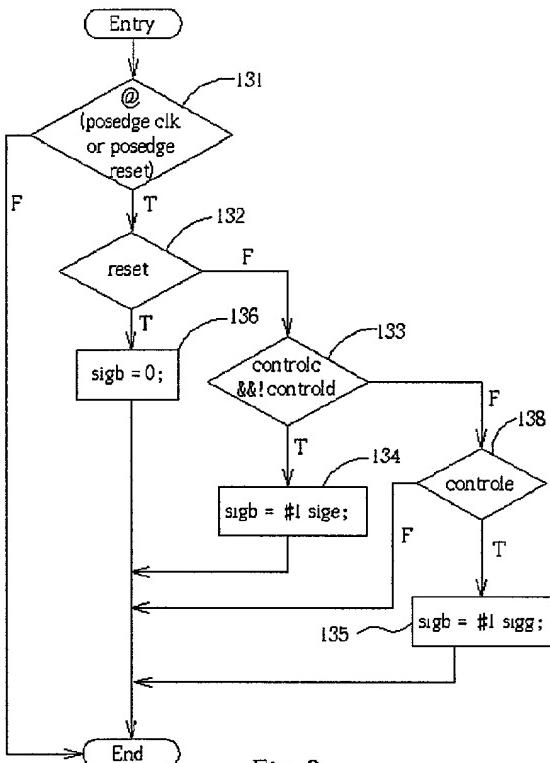


Fig. 9

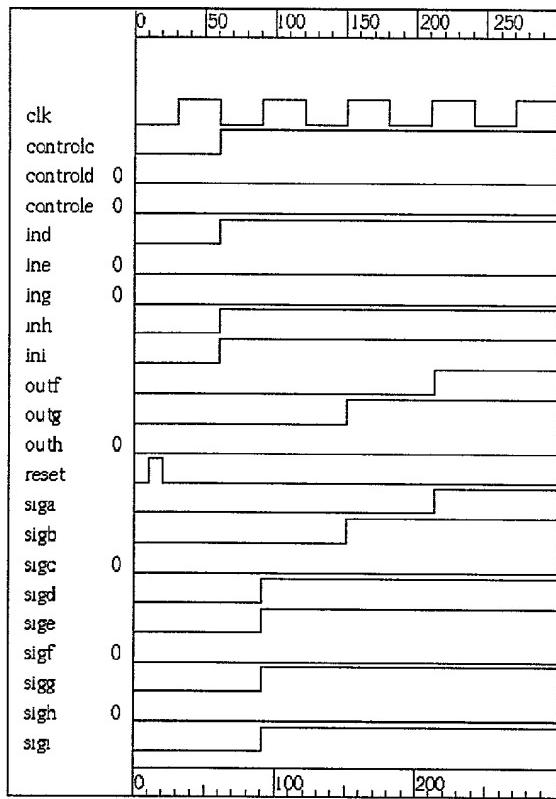


Fig. 10

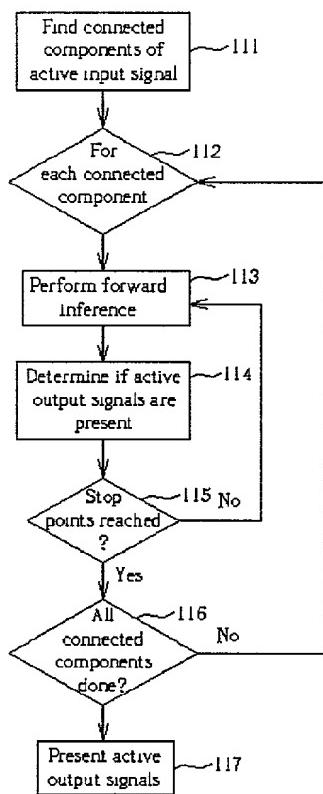


Fig. 11A

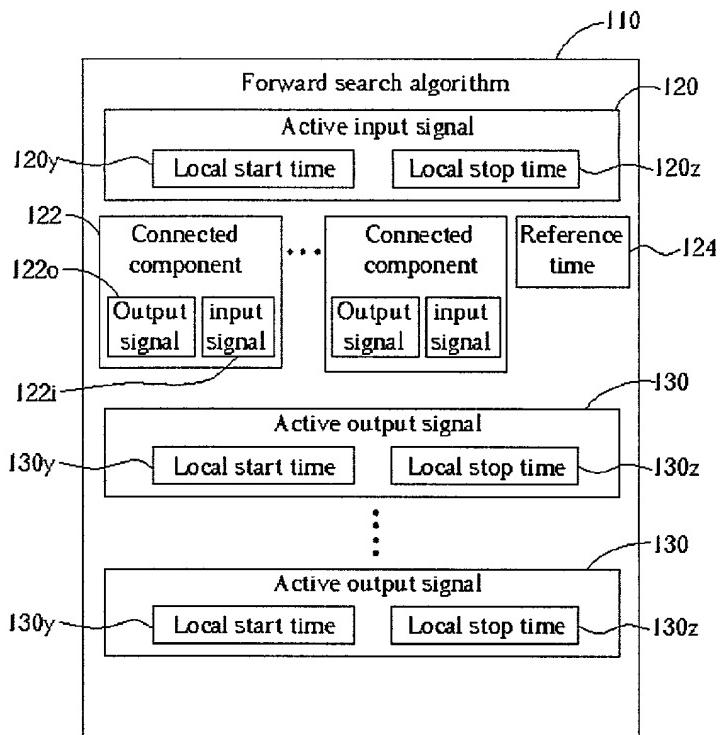


Fig. 11B

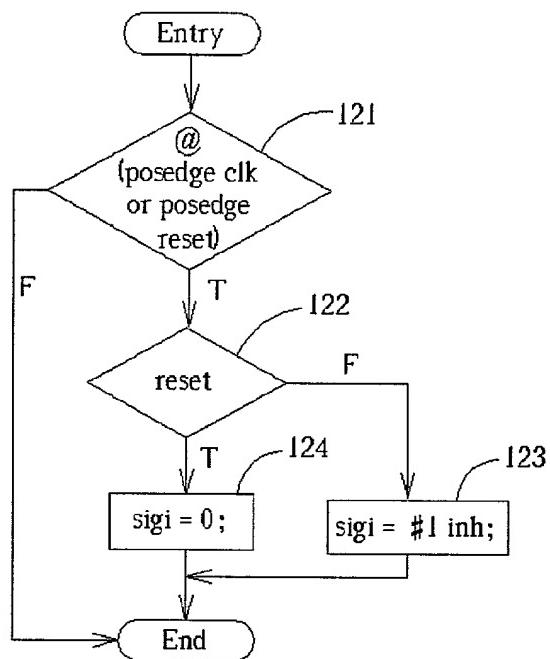


Fig. 12

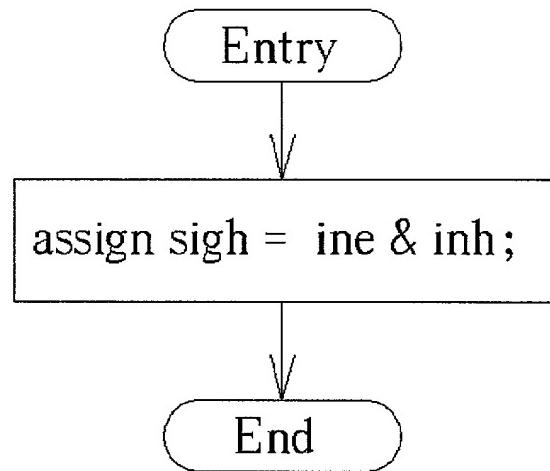


Fig. 13

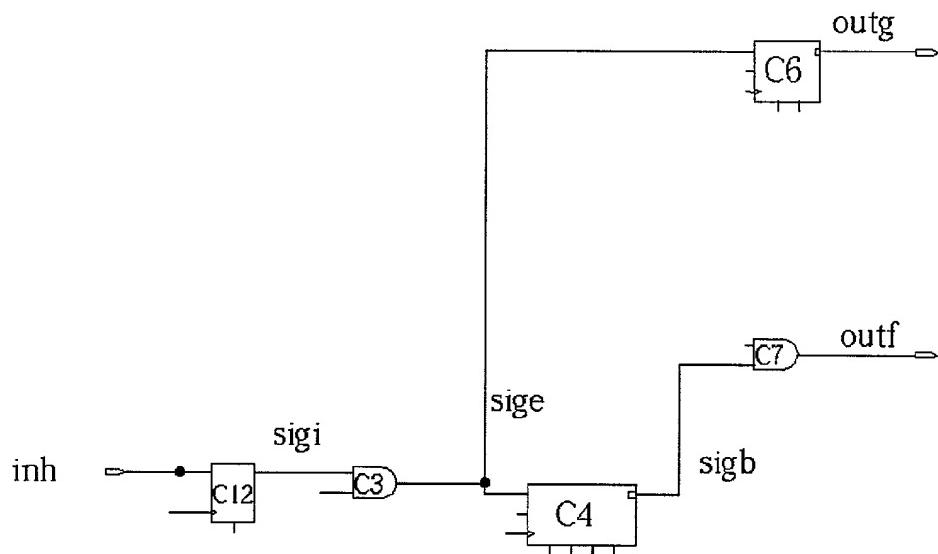


Fig. 14A

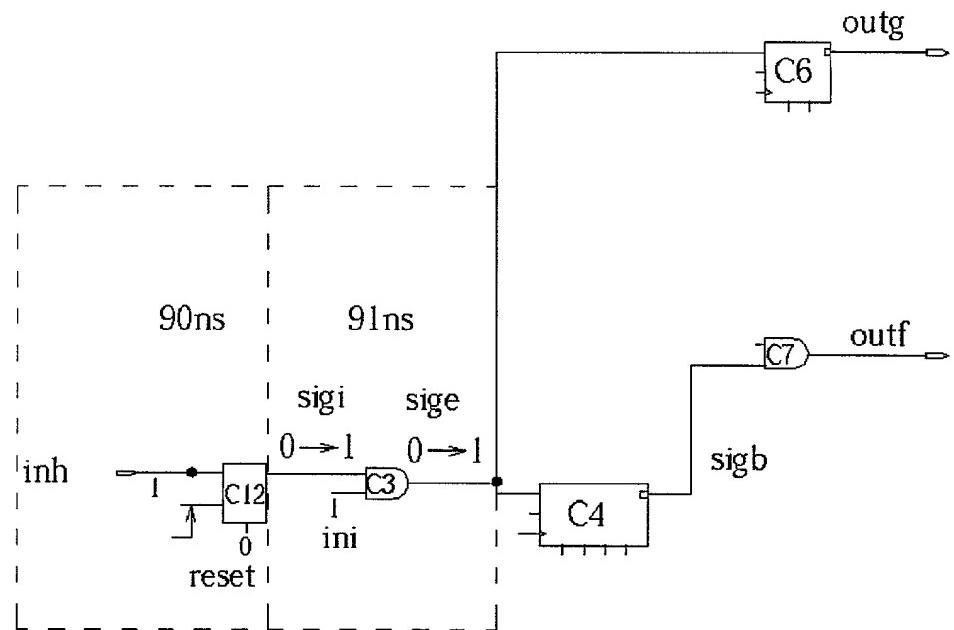


Fig. 14B

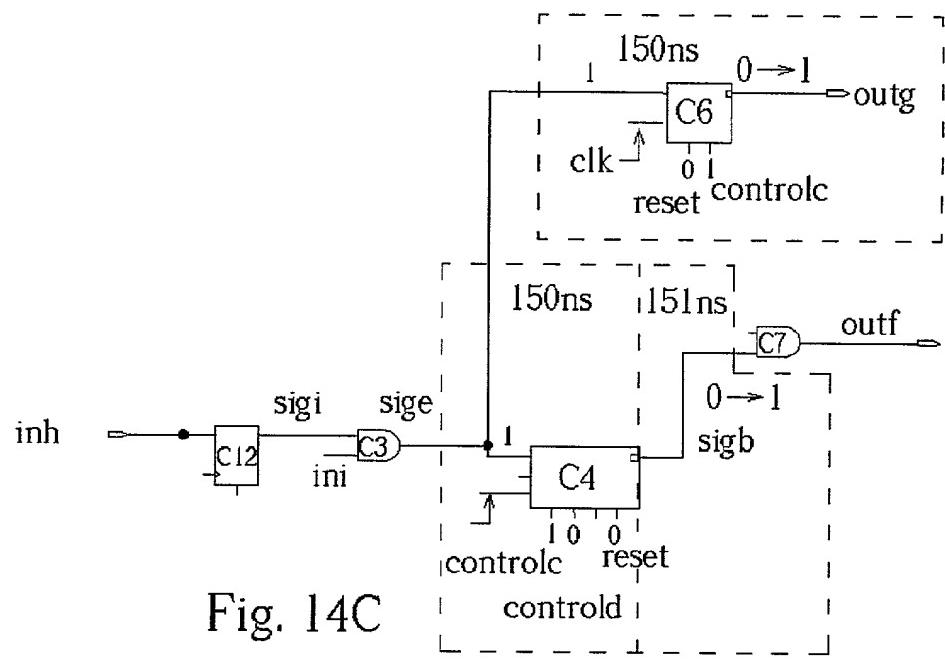


Fig. 14C

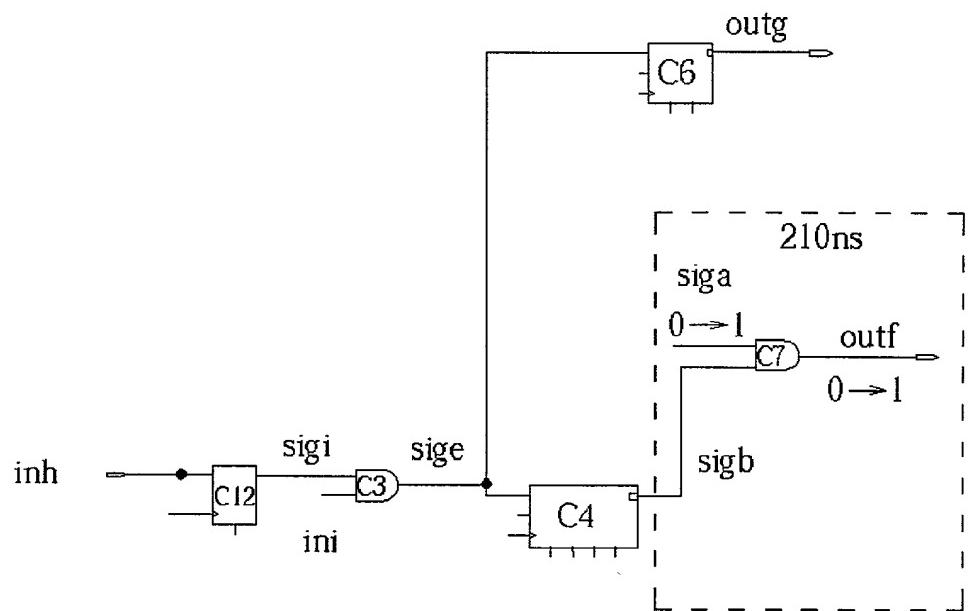


Fig. 14D

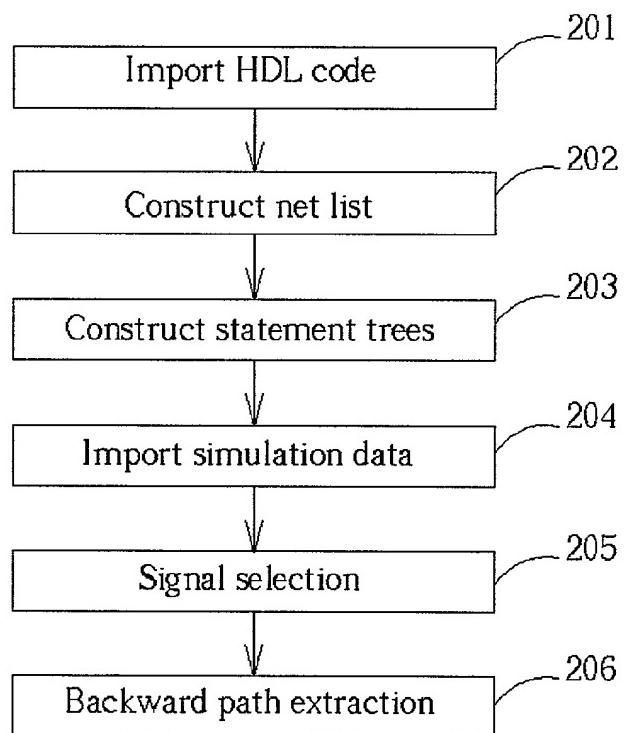


Fig. 15

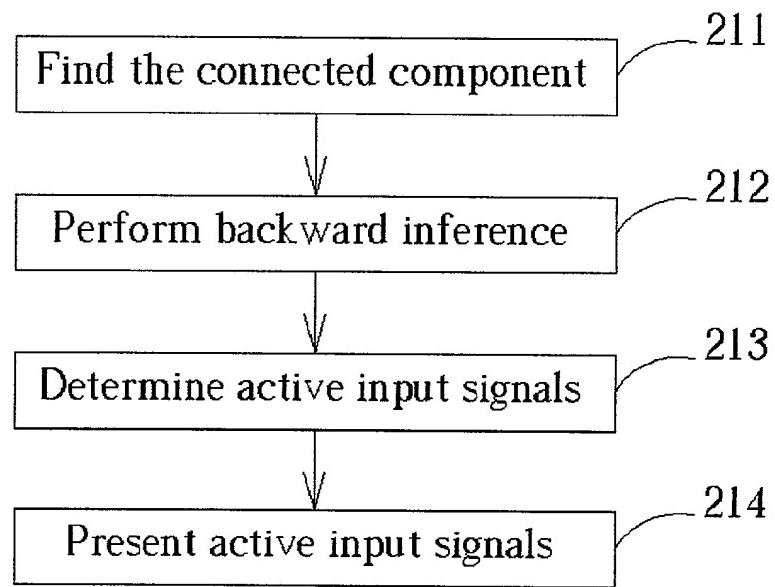


Fig. 16A

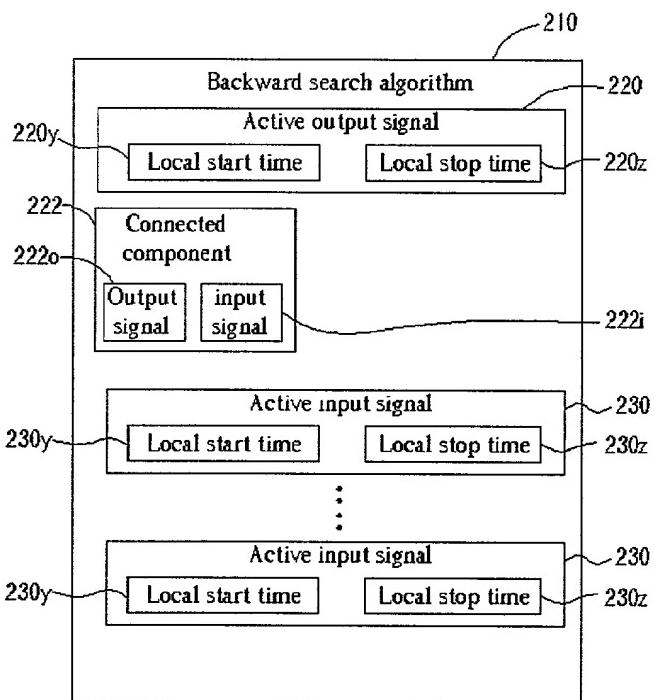


Fig. 16B

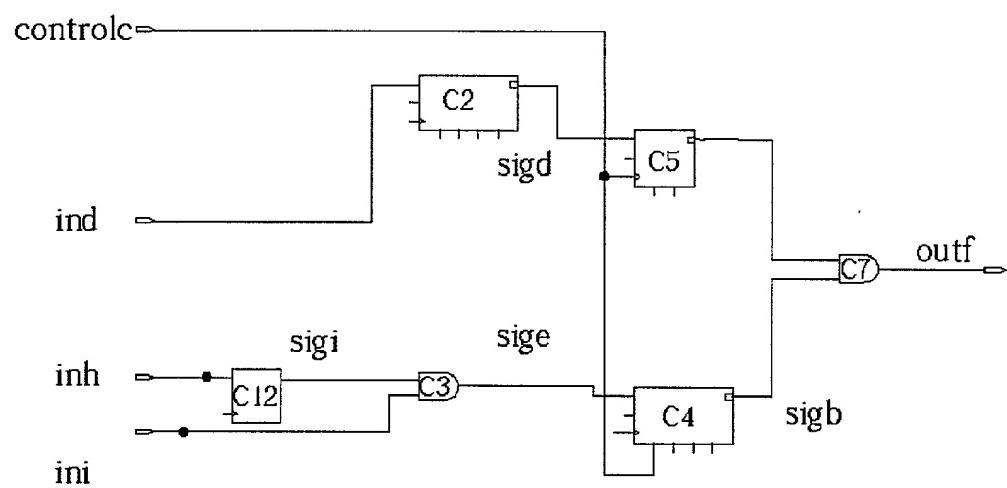


Fig. 17

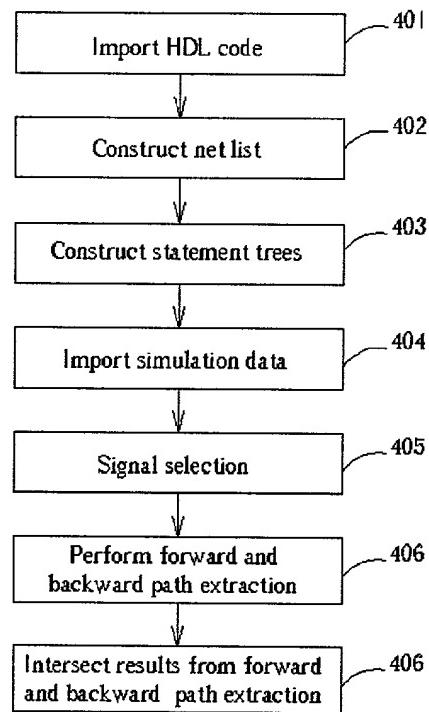


Fig. 18

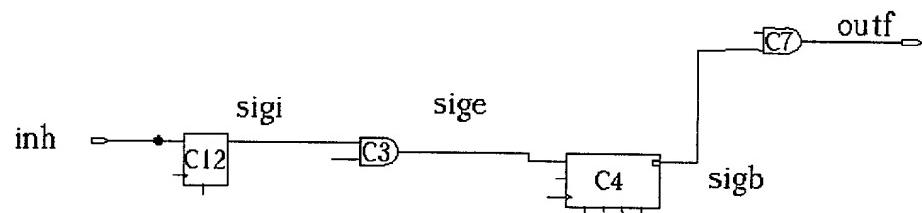


Fig. 19